Special Interest Group

Platform Conference

San Jose January 23-24, 2001 • Taipei February 14-15, 2001

What is the future of ACR ?

Broadband, Wireless and beyond the Integrated Packet Bus

Name: Conrad A. Maxwell

Title: Manager, Product & Technology Planning

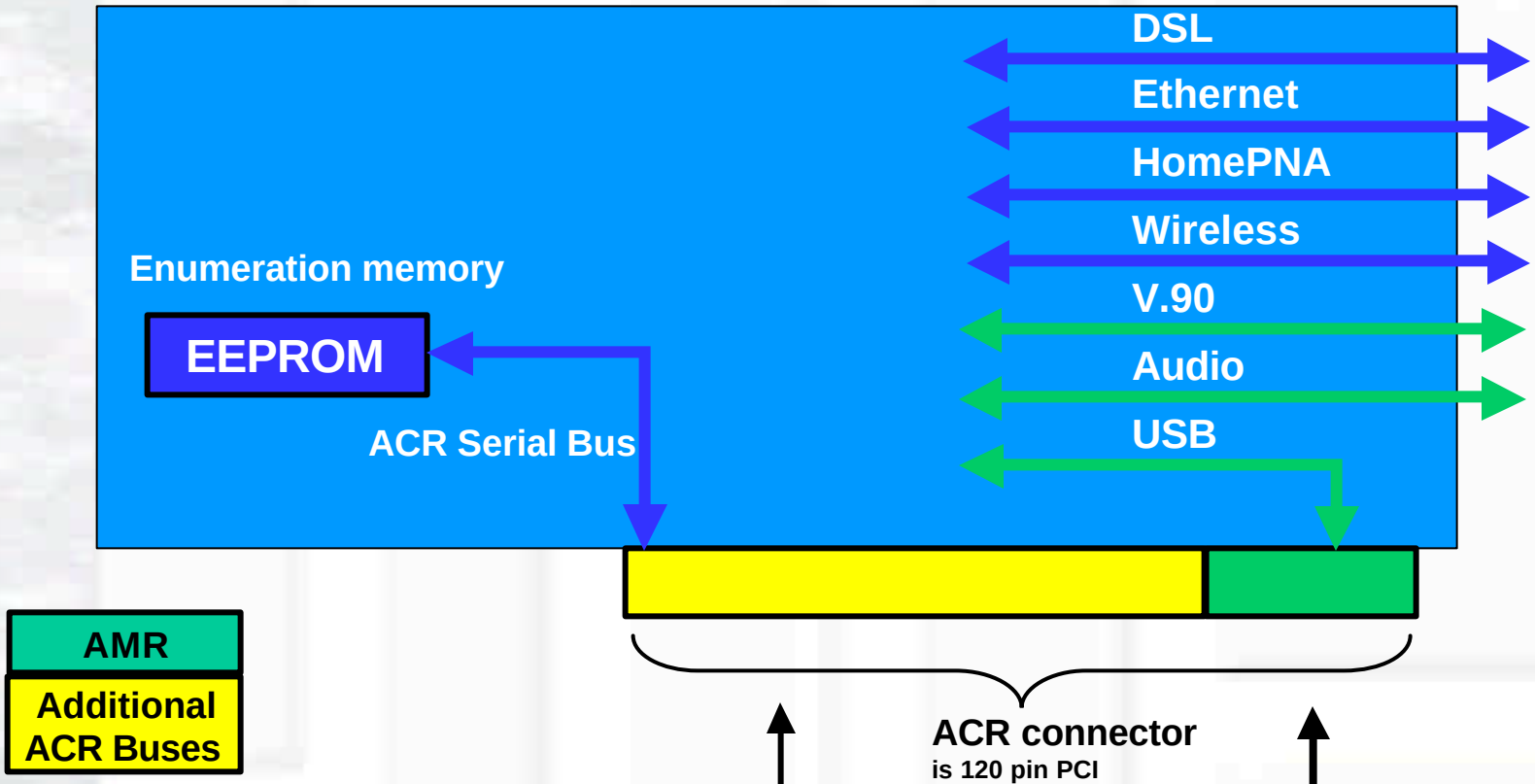
Company: Conexant Systems, Inc.

Taipei : James Wihardja for Taipei

Agenda

- Current Status
- Why do we need IPB ?
- IPB Architecture (Steve Strauss)
- Enhancing Broadband (IPB 2.0)
- Adding Wireless (ACR 2.0)
- Summary

ACR Concept Diagram



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ACR Current Progress

- Last Generation Core Logic
  - Core Logic provides AC-Link Controllers (Audio/Modem)
  - Limited USB port (two)
- Today's Generation Core Logic
  - Multiple Core Logic Devices with a 802.3 MAC
  - The new chips support direct to MII connections
  - The new chips have four (4) or more USB ports
- ACR risers exploit 802.3 combo savings
  - LAN and Modem combos
  - LAN, Modem and Audio combos
  - These combos replace Dual and triple PCI cards
  - Can share RJ11, if MAC is used for HPNA

ACR Goals for Broadband

- Provide
  - A new bus that supports full rate xDSL
  - Power management support
  - Lower cost broadband solutions
- A protocol
  - Simple easy to implement
  - Flexible architecture
    - Supports accelerated, controller-less or host
    - Supports more than xDSL broadband (Cable …)
- Have spare pins for future enhancements

Why do we need IPB ? (1)

- If we look at AGP
  - The shift to 3D graphics was a strain on PCI
  - The graphics bus traffic affected other devices
  - Their were latency issues with rising bits/pixel
  - A dedicated port was warranted, with memory
- PCI was not ready for full 3D Graphics
  - PCI at 33MHz with 32bits has 1056Mbps
  - Graphics needed 32bits per pixel at 1280x960
  - 4,915,200 bits, 80Hz refresh & 2x for texture
  - 10M x 80 or 800Mbps for full 3D Graphics

Why do we need IPB ? (2)

- If we look at AC Link
  - The Audio and Modem function was redone
  - The bus traffic and latency were not the issue
  - Cost reducing the architecture was the issue
  - A standard interface to codecs was needed
- AC Link is a 48KHz bus
  - 20 bit slot per channel
  - 6 channels for audio
  - 2 channels for analog modem
  - A simple TDM bus protocol was used

Why do we need IPB ? (3)

- If we look at IPB
  - The data rate is 8Mbps for G.dmt
  - There are control streams inside the data
  - 8Mbps is not a good indicator for bus traffic
- The actual load for G.dmt
  - The data is modulated up to 1.1MHz
  - Nyquist sampling states a rate 2.2MHz
  - Adequate resolution requires 16 bits
  - The actual load is ~ 35Mbps for G.dmt
  - Too high for a good USB Client

Why do we need IPB ? (4)

- If we look at VDSL
  - The data rate is 50Mbps
  - There are control streams inside the data
  - 50Mbps is not a good indicator for bus traffic
- The actual load for VDSL
  - The data is modulated up to 8MHz
  - Nyquist sampling states a rate 16MHz
  - Adequate resolution requires 16 bits
  - The actual load is ~ 256Mbps
  - Too high for a good PCI client or USB 2.0

Why do we need IPB ? (5)

- Summary
  - IPB shares issues with AC Link and AGP
    - Like AC Link, IPB enables lower cost designs
    - Like AGP, IPB provides a dedicated bus
  - If we look at broadband today
    - The actual load strains USB
    - A dedicated bus insures robust performance
  - If we look at broadband tomorrow
    - The actual load strains PCI or USB 2.0
    - The need for a dedicated bus become clear
  - To scale from now into tomorrow use IPB

Why do we need IPB ? (6)

- Graphics drove AGP
- Cost reduction drove AC Link
- Broadband is driving IPB
  - Better system performance
  - Cost reduction

IPB Architecture

the Integrated Packet Bus

- Steve E. Strauss from Lucent

IPB Architecture and Uses

Supporting Broadband Connectivity- the Integrated Packet Bus(IPB)

Steven E. Strauss
Distinguished Member of Technical Staff
Agere Systems- formerly the Microelectronics Group of Lucent Technologies

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Introducing IPB 1.0

- Designed to meet the requirements for the next generation of communication bus for the PC industry
  - Developed in tandem with the ACR specification
- High-speed (up to 80 Mbps) data transport
  - enables host CPU to directly process the communications stream
  - offers high speed data transfers in a variety of hardware and software core combinations
  - Allows OEMs the flexibility to implement communications solutions across a wide range of the performance and cost spectrums

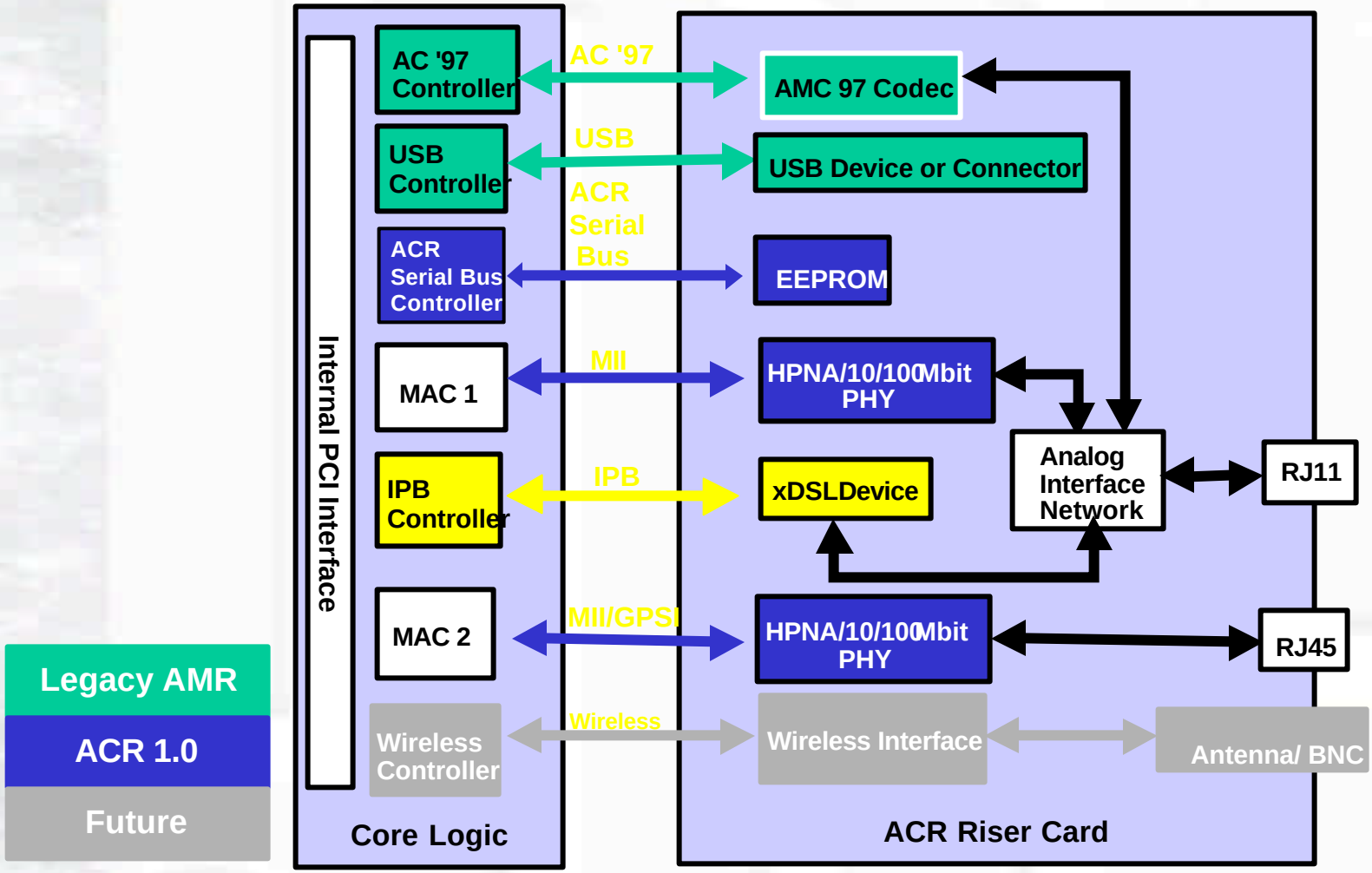
Introducing IPB 1.0

- The IPB defines a transport mechanism with a structured protocol but not device functionality
  - Provides standardized link architecture, regardless of the type of protocol used: G.Lite, xDSL, Cable Modem, etc.
- Improves robustness beyond PCI solutions

Adding Broadband

- Provides
  - A new bus that supports full rate xDSL
  - Power management support
  - Lower cost broadband solutions
- A protocol
  - Simple & easy to implement
  - Full Duplex Time Division Multiplexing (TDM) design
    - status and control slots at the beginning and end of each frame
  - Flexible
    - Supports accelerated, controller-less or host architectures
    - Supports more than xDSL broadband (Cable …)
  - similar to AC97

ACR Architecture



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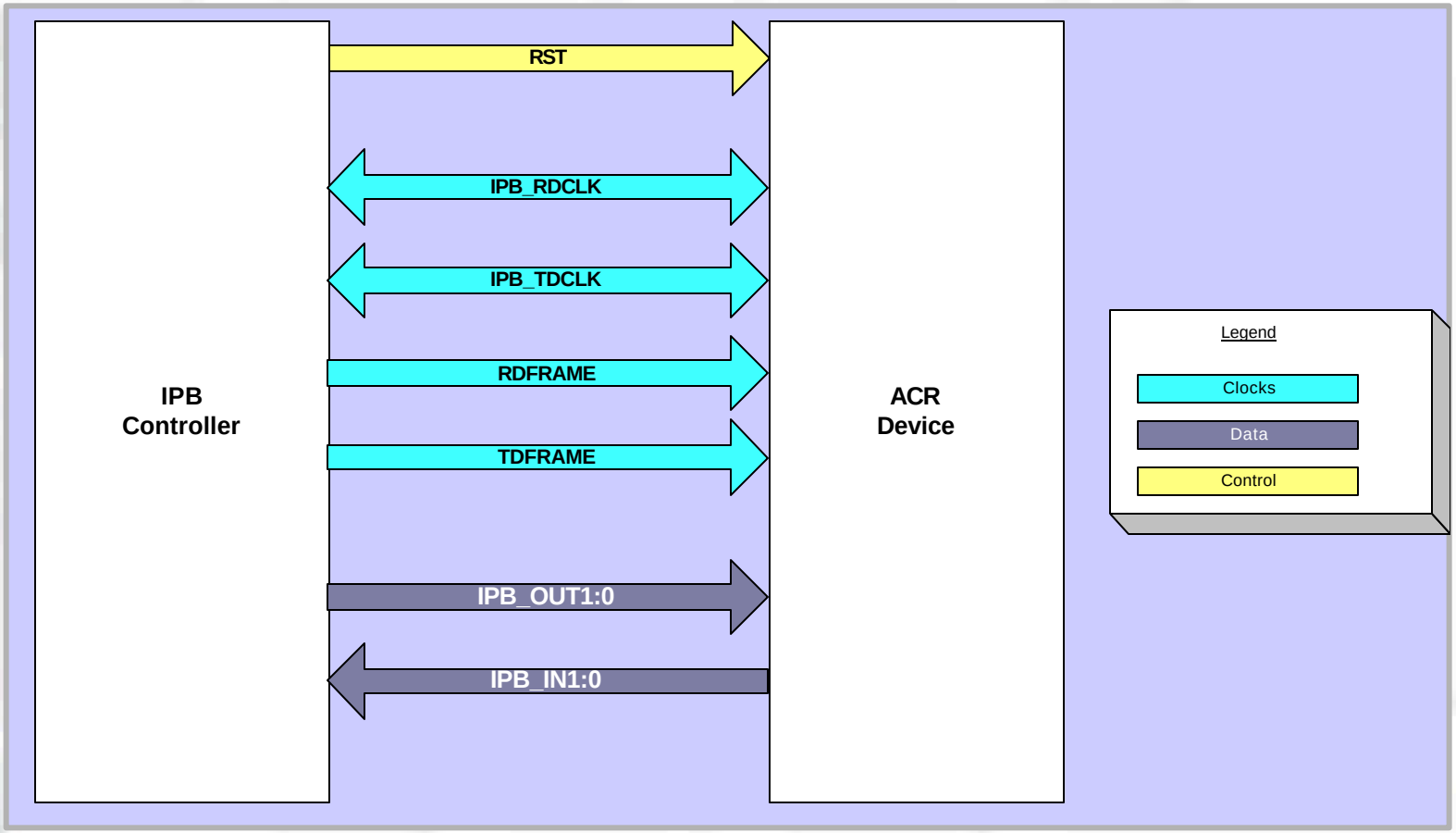
IPB Architecture



The IPB bus consists of a clock signal for each direction of transfer (TDCLK and RDCLK), two data bits in each direction (IPB_IN[1:0] and IPB_OUT[1:0]) and up to two framing signals (RDFRAME and TDFRAME).

IPB has advantages over AC Link & PCI

- AC Link is not enough
  - Only two modem slots were defined and full rate xDSL is too fast (20x48Kx2=1.92Mbps)
  - Concurrency with V.90/V.92 would be lost
- PCI adds complexity
  - Riser PSTN I/O will require RJ11 jumper wires
  - PCI is a larger form factor than riser cards
  - PCI requires more pins to support the chip interface
  - PCI has a lower memory access profile for DMA

A Simple TDM Protocol

- The protocol accommodates ATM packets
- The IPB protocol has a data slots and embedded control slots for simultaneous control and data transfer
- Data slots
  - Can be used as needed for dynamic expansion of broadband speeds
  - Can be altered for optimum QoS delivery (latency)
- It could be described as a bigger and better AC Link or maybe DSLink™ or Cablink™

The TDM Protocol in Detail

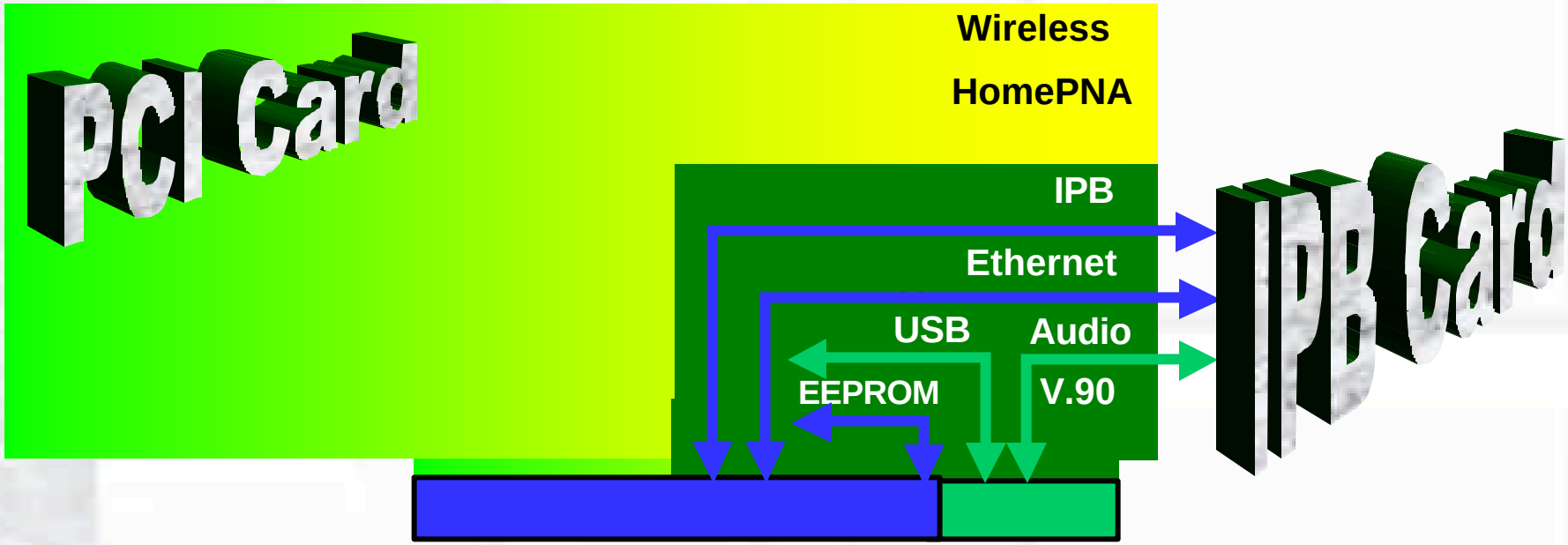
- Frame length is programmable
- The bus is full duplex bus with two data pins
- Frame rate is programmable

The TDM Protocol

- The memory access improves latency
  - Memory arbitration logic for high priority allocation
  - This does not allocate bandwidth directly
- There are bits for flow control in the protocol
  - Tagging valid packets
- The packet flow can be optimized for the pipe
  - Frequency of frames
  - Data payload size
- The combined affects provide a more robust access to memory

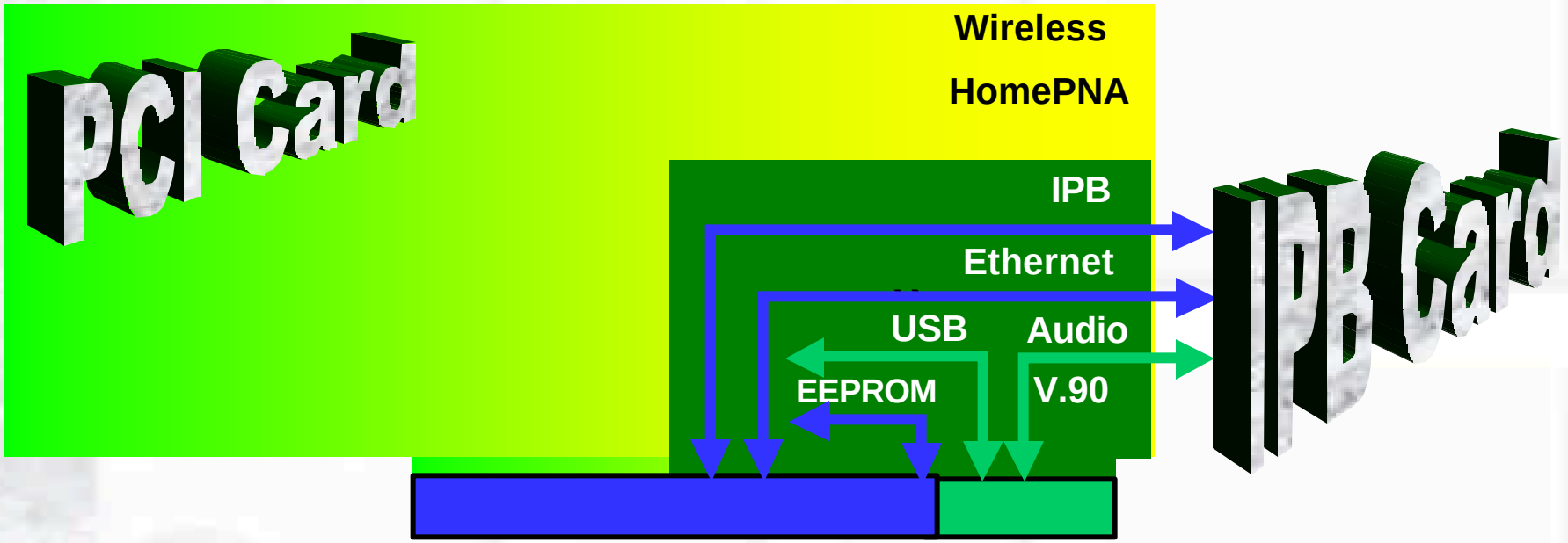
Mechanical Considerations

- IPB uses only a portion of the PCI connector
  - IPB risers are smaller than PCI cards

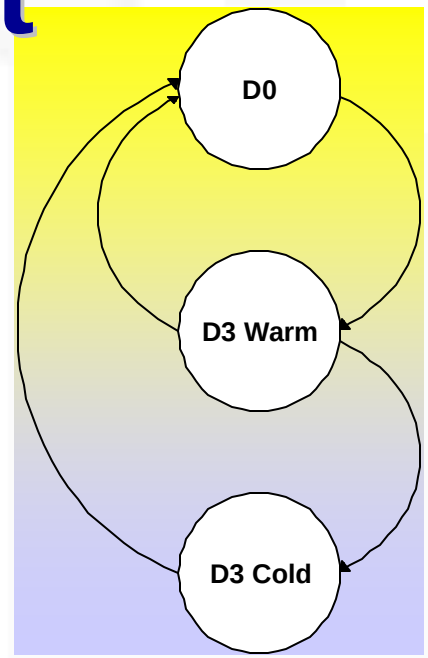


Electrical Considerations

- IPB was defined for 3.3Vdd devices
- Other voltages are present for analog on ACR
  - +12V/ -12V, +5V and isolated power and grounds per bus

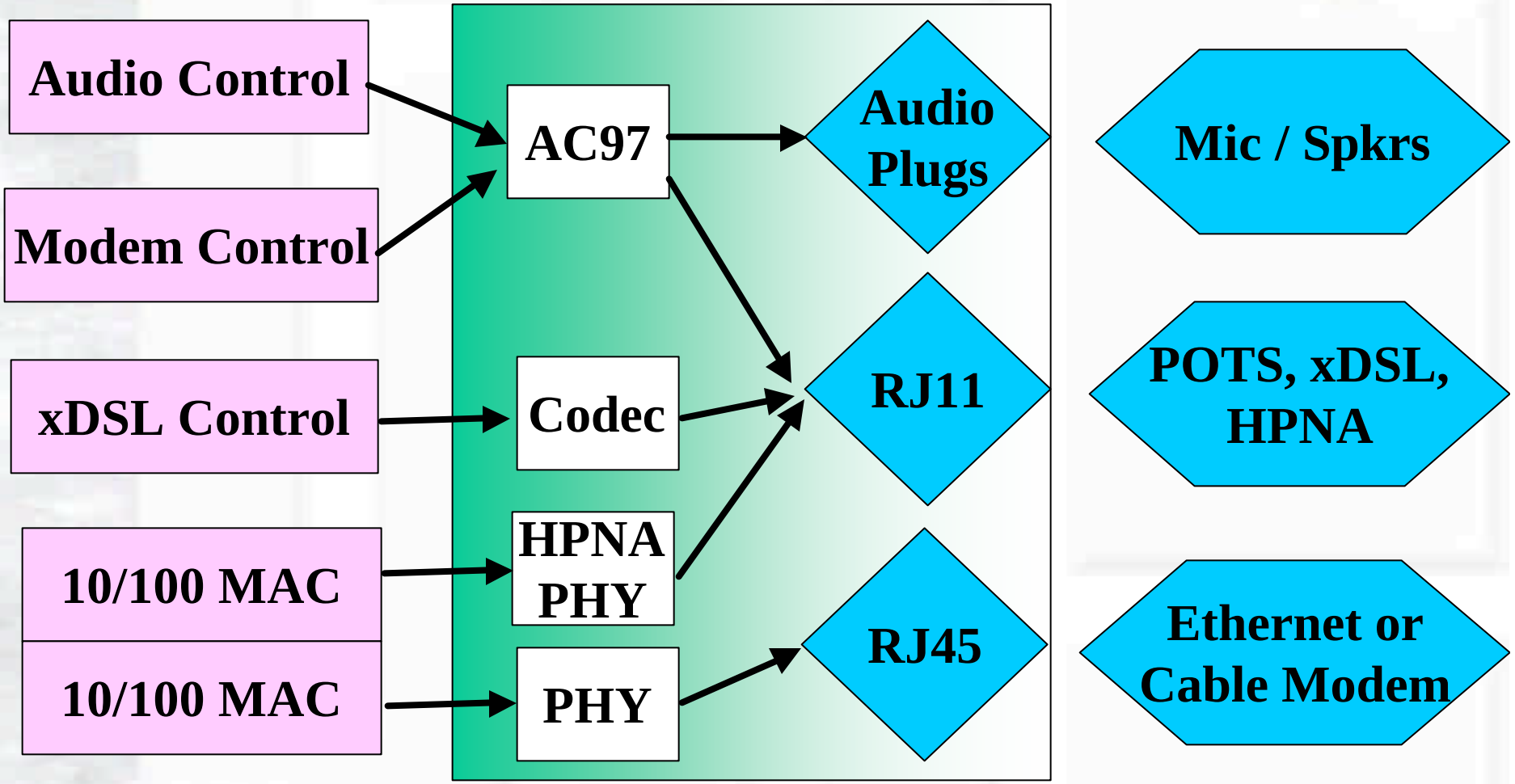


IPB Power Management



- IPB requires three states
  - D0 - normal mode (ON)
    - Required clocks and sidebands enabled
  - D3 - warm (device disabled, power ON)
    - Required clocks and sidebands disabled
  - D3 - cold (device power OFF, Aux ON)
    - Use cold reset and configuration to restart
- Controller must retain info except for D3 cold
  - Can restore operation without a configuration cycle
- Wake on event in D3 cold supported
  - Aux power used on physical layer (“always on”)

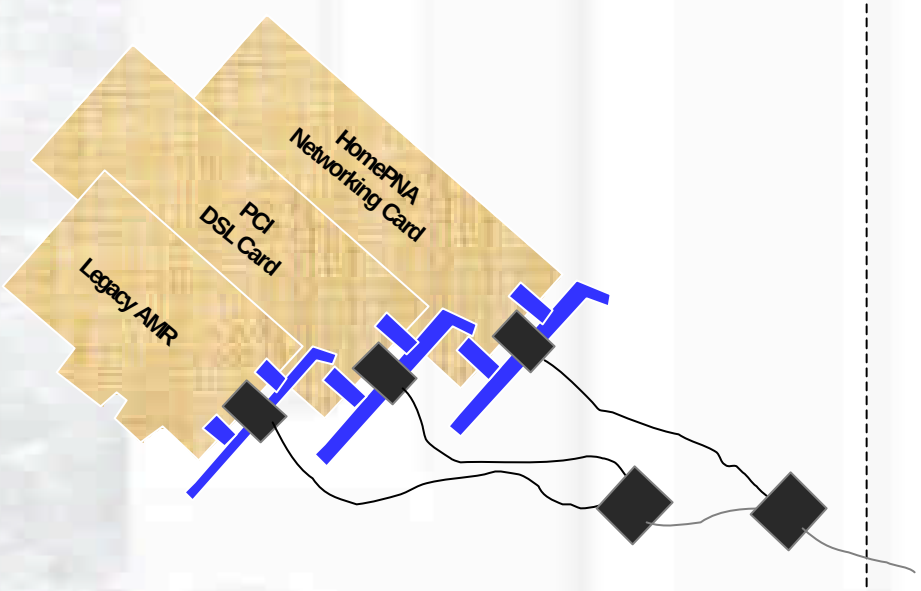
ACR Block Diagram

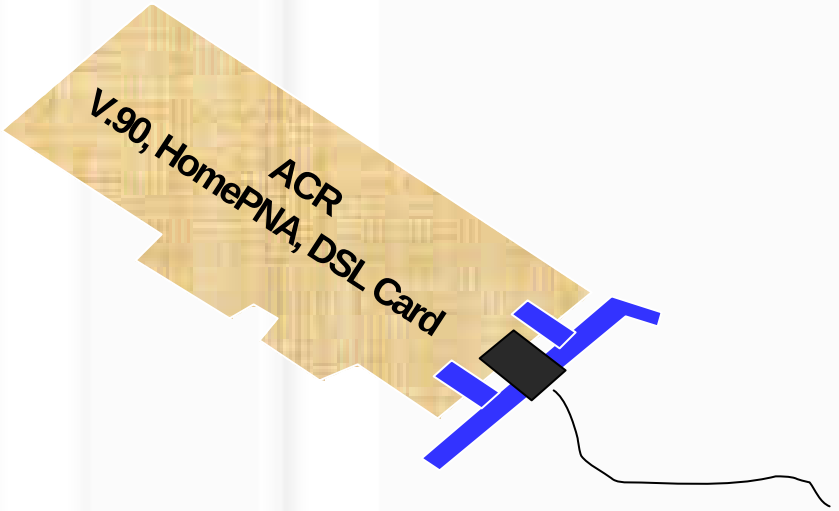


DSL and RJ11 connections

Legacy Designs

- Need separate cards for each phone line function and require adapters to merge the lines into one combined phone wire





ACR Designs

- Combine all the phone line functions on a single card that uses a single RJ-11 connector

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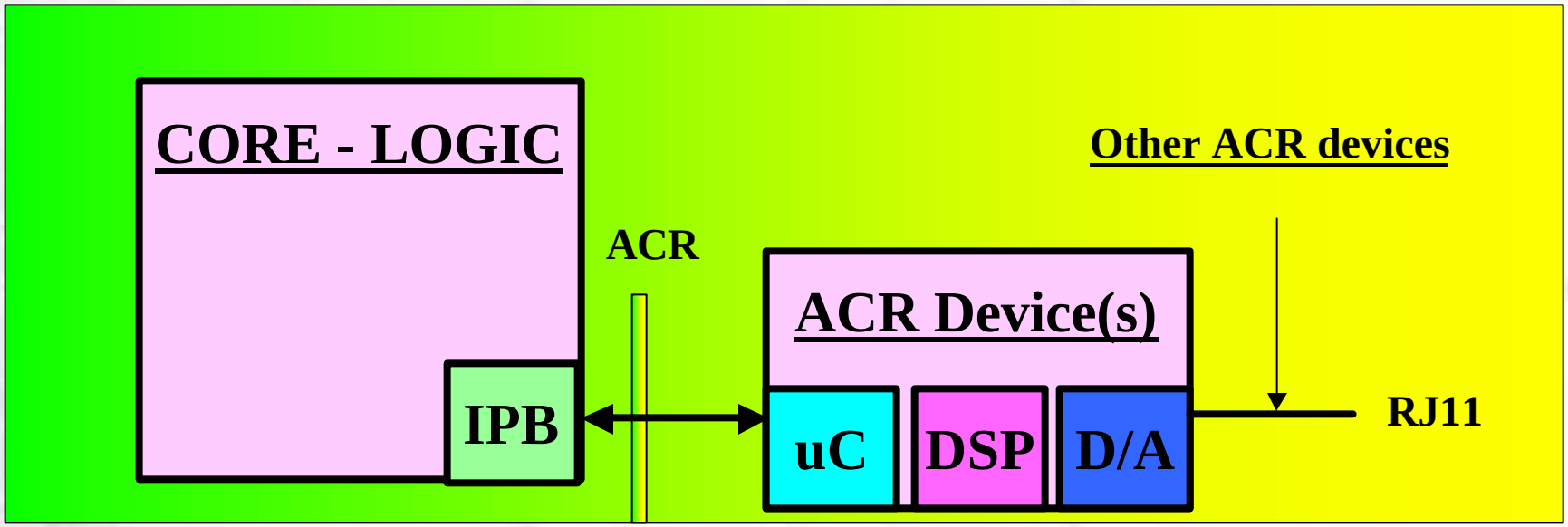
IPB Support for Broadband

- IPB high-speed data transport enables:
  - Accelerated Broadband
  - Controllerless Broadband
  - Host Based Broadband
- System architecture and processing power continue to evolve
  - allows system CPU to process most of the communications stream directly
  - allows low cost CODEC type interface to the analog data stream to be developed

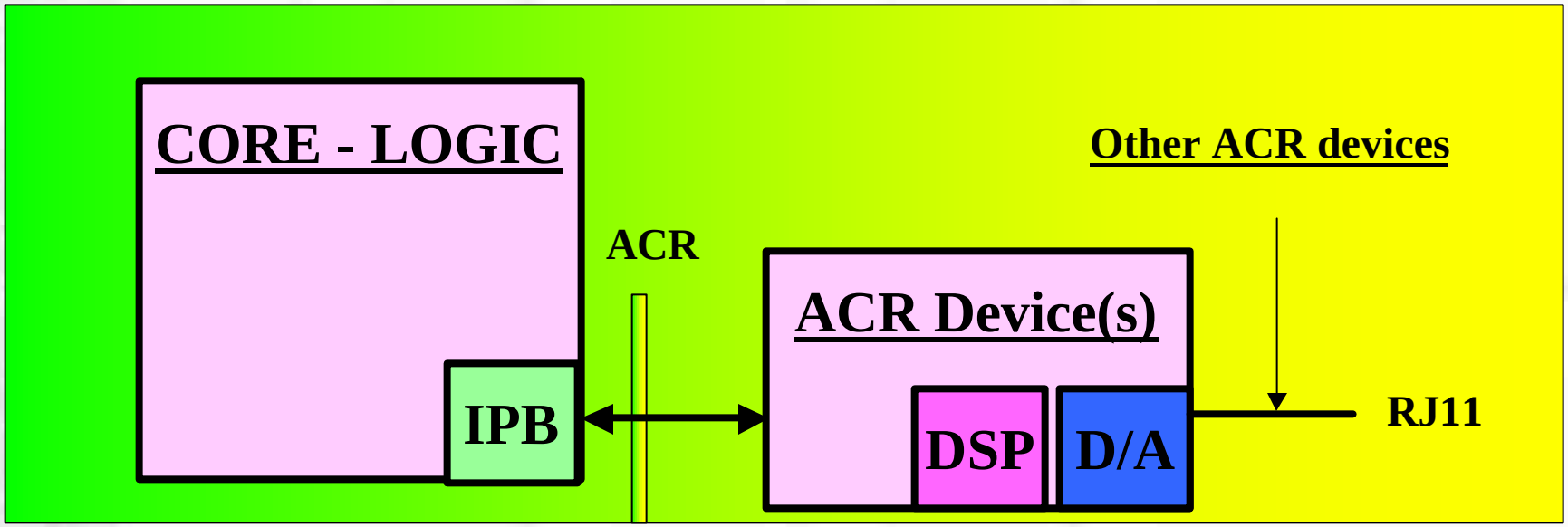
IPB & Accelerated Broadband

- Low to zero host impact
- The IPB host drivers are just pass-thru
- Control, signal processing and conversion



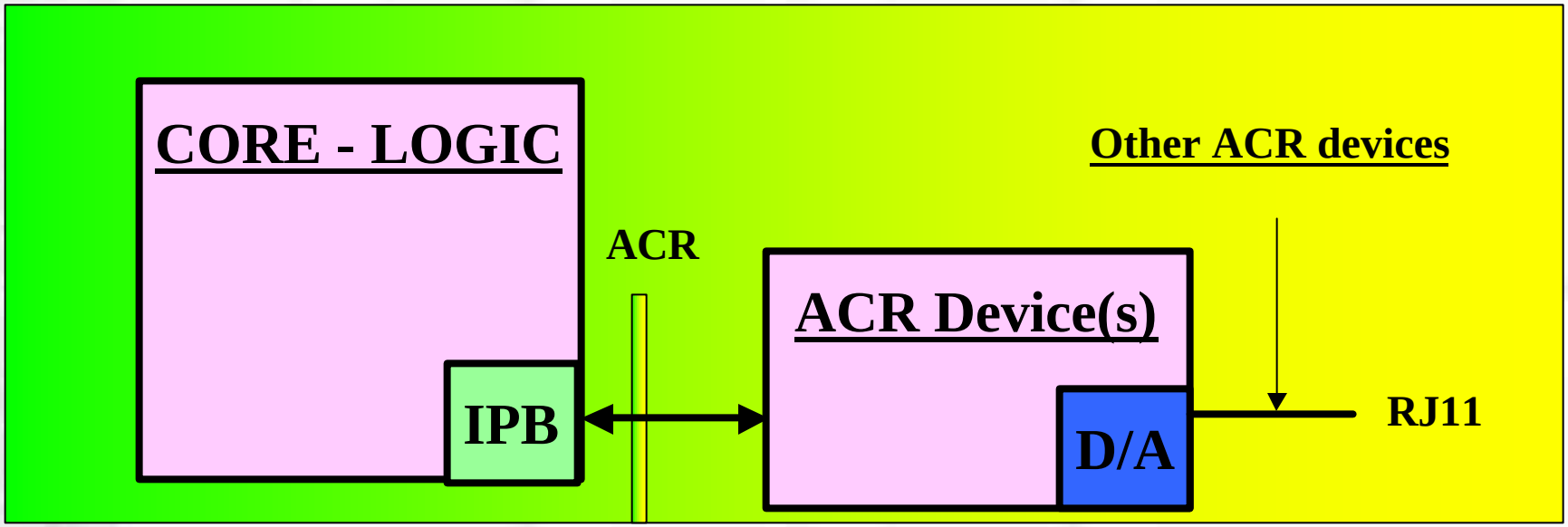
IPB & Controllerless Broadband

- Medium host impact
- The IPB host drivers provide control
- Signal processing and signal conversion



IPB & Host Based Broadband

- Higher than Medium host impact
- The IPB host drivers, control and DSP
- Signal conversion



IPB Conclusions

- IPB supports the requirements for next generation high-speed peripherals
  - defines a transport mechanism with a structured protocol
  - Designed to support robust and interoperable product implementations
- IPB is coming to a broadband connection near you…
  - Interface is available in initial version of the specification
  - Broadband technology-based products are being developed and will be introduced into the marketplace that will leverage IPB
  - Data rate improvements and other advances (such as DDR) will be addressed in future revisions of the specification

Advanced Communications Riser

www.acrsig.org
email: info@acrsig.org

email: sstrauss@agere.com

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ACR Future Progress

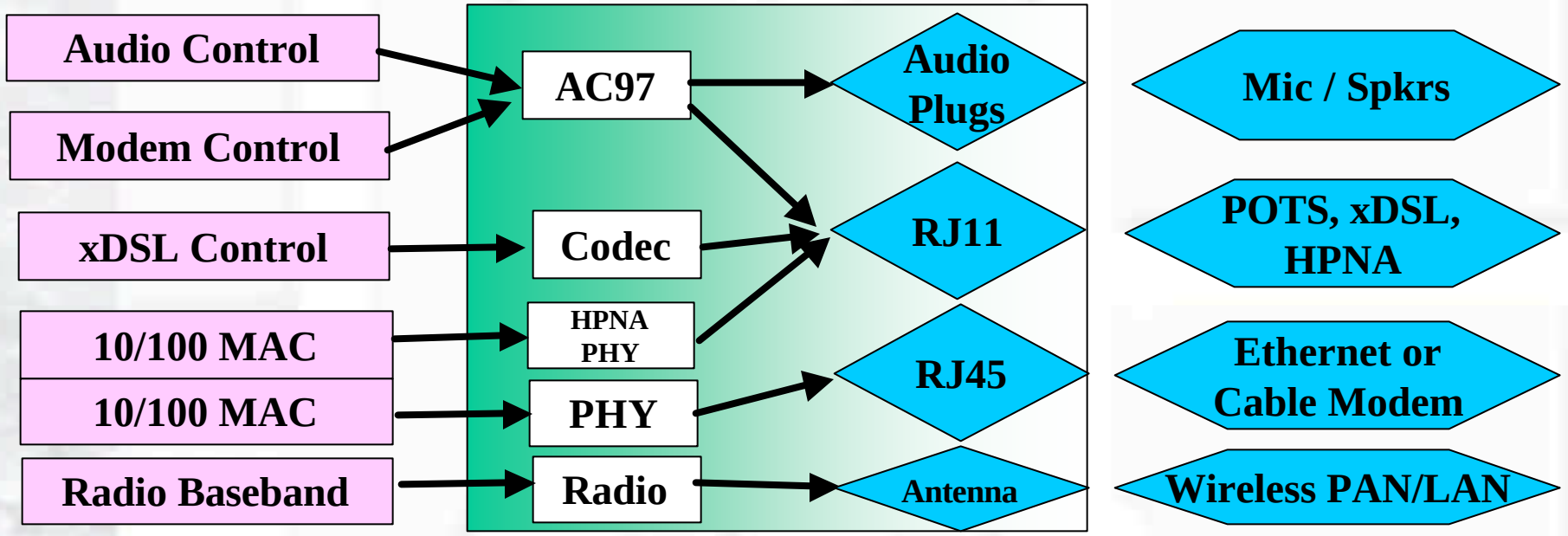
- Next Generation Core Logic
  - Will support broadband using IPB controllers
  - The controller will be integrated
- IPB is part of ACR 1.0 Today
  - Designs are underway
  - First Half 2001 - will be the first samples
  - Softer DSL will lower broadband chip count
- Wireless radios use a fast serial I/F
  - ACR 2.0 will add a standard serial bus
  - This bus will enable softer baseband designs

ACR Future Progress

- IPB 2.0 is part of ACR 2.0
  - Performance will be enhanced
  - late 2002 is the target for first samples
  - Softer VDSL will lower broadband chip count
  - Faster CPU's will not be idle - broadband code
- IPB can support more than xDSL
  - Wireless radios
  - HPNA
  - Homeplug
  - Cable modem AFE/PHY
  - and many more ...

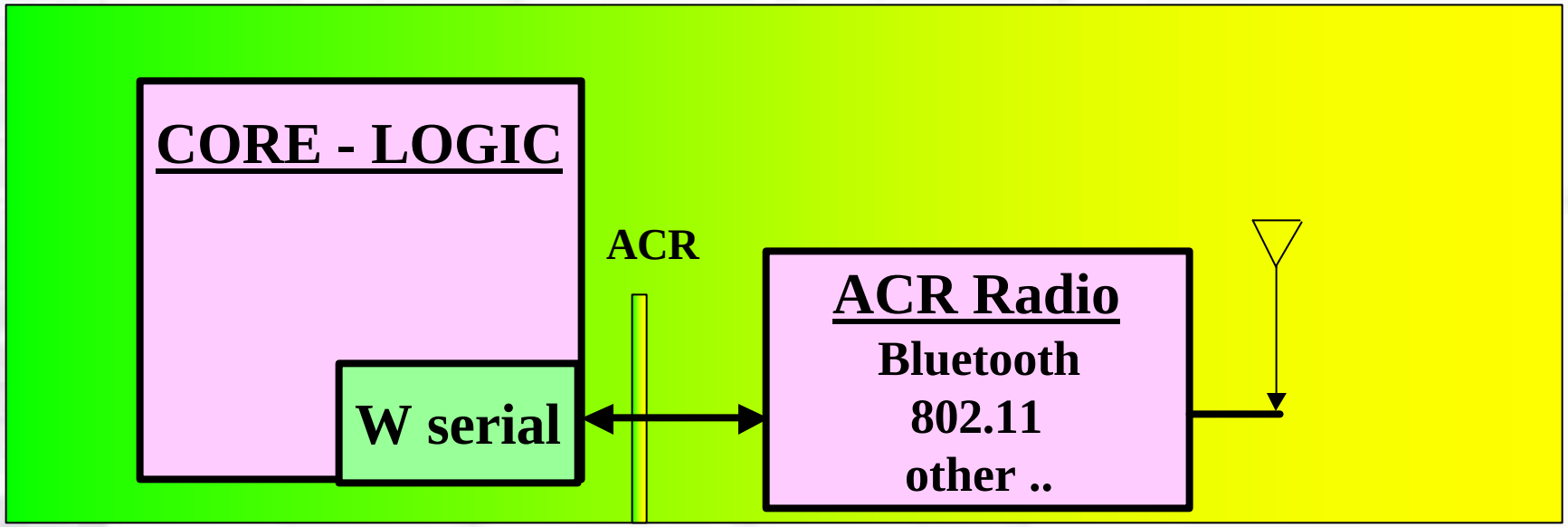
Adding Wireless

- ACR.Lite provides Audio and POTS modem
- The MII buses add LANs (10/100 & HPNA)
- The high-speed internet connection on IPB
- Second LAN choice Wireless Future Bus



Wireless on ACR 2.0

- Host code baseband controller
- The radio uses host drivers
- Serial Radio is the only device



Summary

- ACR 1.0 supports:
  - Improved PnP for AC Link (EEPROM)
  - Two LAN ports (MII)
  - One broadband port (IPB)
  - Legacy AMR
  - No new connector for MB
- ACR 2.0 will support
  - Enhanced IPB
  - Wireless serial port

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www.acrsig.org email: conrad.maxwell@conexant.com
email: info@acrsig.org

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